MASTER/SLAVE SYNCHRONIZATION COMMUNICATION SYSTEM

Background of the Invention

Field of the Invention

[0001]

5   The present invention relates to a communication system for a real-time control system that performs master/slave synchronization communications by using IEEE1394.

Description of the Related Art

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[0002]

In a related art of the master/slave synchronization communication system, similar to PROFIBUS-DP, a master simultaneously broadcasts a data packet notifying the

15   synchronization point of a communication period and each slave detects the synchronization point with its reception timing, and instruction data is thereafter exchanged with response data by way of polling (For example, refer to Non-patent Publication 1.).

20   [0003]

In another system such as SERCOS (Registered Trademark), a master simultaneously broadcasts a data packet notifying the synchronization point of a communication period and then transmits instruction data to

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each slave while each slave sequentially transmits response data after a predetermined period has elapsed since the synchronization point or based on a predetermined transmission order (For example, refer to Non-patent

5 Publication 2.).

[0004]

Such a system where a master and slaves communicate with each other in synchronization is a general communication system used in a real-time control system.

10 [0005]

An IEEE1394-compatible network is a high-speed general-purpose network generally used by a personal computer or an AV device. Its transmission speed is 100Mbps to 3.2Gbps, which ensures extremely high-speed

15 communications compared with PROFIBUS-DP whose highest speed is 12Mbps and SERCOS whose highest speed is 16Mbps. The IEEE1394-compatible network has features not available from the Ethernet (Registered Trademark) which is also a general-purpose high-speed network: isochronous

20 communications are supported where all nodes connected to the network operate at a natural period of 125 μ s. Application of such a network to a network for real-time control that performs the master-slave synchronization communication is expected (For example, refer to Patent

25 Publication 1.).

[0006]

Fig. 12 shows a communication time chart of a communication system generally used in PROFIBUS-DP or the like. In Fig 12, signs c1, c2,… represent instruction data timings a slave #1, a slave #2, and so on while signs r1, r2,… represent response data transmission timings from the slave #1, the slave #2, and so on. As shown in Fig. 12, a synchronous packet is simultaneously broadcast at a synchronization point at the head of a communication period and then instruction data is transmitted to the slave #1, slave #2, and so on. On receiving the instruction data, the slave #1 returns response data. On receiving the instruction data, the slave #2 returns response data. In this process of so-called polling, instruction data and response data are transmitted/received until another synchronization point is reached after the communication period has elapsed when a synchronous packet is simultaneously broadcast.

[0007]

Fig. 13 shows a communication time chart of another communication system employed in SERCOS or the like. As shown in Fig. 13, a synchronous packet is simultaneously broadcast at a synchronization point at the head of a communication period, same as the case in Fig. 12. Following this, instruction data c1, c2,… to be transmitted

to the slaves is transmitted with a timing from the master, sometimes in a single packet. After a predetermined time value adjusted per slave has elapsed, the response data (r1, r2,…) is transmitted until another synchronization point is reached after the communication period has elapsed when a synchronous packet simultaneously broadcast.

[0008]

In this way, in the related art of the master/slave synchronization communication system, a synchronous packet is simultaneously broadcast at every synchronization point of a cc period in order to assure synchronization of all stations.

[0009]

Patent Publication 1: JP-A-2003-008579

Non-patent Publication 1:PROFIBUS-DP   Specification (IEC61158 Type3)

Non-patent Publication 2:SERCOS   Specification (IEC61491)

Summary of the Invention

[0010]

However, the related art of the master/slave synchronization communication system requires operation where a synchronous packet is simultaneously and accurately broadcast at every synchronization point from a master to

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notify each slave of a synchronization point. In the case
where the isochronous communications of an IEEE1394-
compatible network are applied in order to support this
request, a cycle start packet edited and simultaneously
5   transmitted per natural period is the most ideal
synchronization point notification section although the
packet does not guarantee the transmission timing accuracy
thus causing jitter at a synchronization point.

[0011]

10   Another problem with the related art of the
master/slave synchronization communication system is that
the natural period is fixed and cannot be modified even
when it is necessary to provide a communication period
longer than the natural period because of an increased
15   number of slaves.

[0012]

The isochronous communication of IEEE1394 is a
communication system where packets are simultaneously
transmitted with difficulty in adjustment of data
20   transmission timing to the transmission path as well as no
assurance of transmission order. This makes it difficult
to perform polling used in the related art of the
master/slave synchronization communication system or data
transmission scheduling after a predetermined time since a
25   synchronization point or in accordance with a data

transmission order.

[0013]

In the case of JP-A-2003-008579 cited as a related art, a unique trigger packet (synchronous packet) is simultaneously broadcast instead of a cycle start packet via isochronous communications and each slave performs data communications via asynchronous communications to make a transmission request from a master in order to secure a communication period across multiple isochronous cycles. This results in greater jitter. Moreover, switching between isochronous communications and asynchronous communications complicates communication processing in each station.

[0014]

The invention has been accomplished in view of the problems. An object of the invention is to provide a master/slave synchronization communication system that applies IEEE1394, and uses its natural period as a base cycle so as to provide synchronization of all stations with a communication period as an integral multiple of the base cycle, thereby allowing easy scheduling of data transmission/reception.

[0015]

In order to attain the object, the first invention described in claim 1 provides a master/slave

synchronization communication system, having: a single master and a single or a plurality of slaves that are based on IEEE1394, wherein the master/slave synchronization communication system has a communication period which is set to an integral multiple of a natural period of IEEE1394 communications with the natural period considered as a base cycle, each of the master and the slaves has a detecting section of a synchronization point being a start timing of the communication period, and a base cycle counter which shows what base cycle number the present cycle is from the synchronization point, the master has a transmission management table in which destination slaves of instruction data are previously allocated to each of the base counter values and transmits instruction data to each slave every time the base cycle counter is updated based on the transmission management table, and each of the slaves transmits response data to the master when the pre-allocated value of the base cycle counter is reached.

[0016]

In this way, it is possible to perform data communications based on a base cycle counter thereby performing synchronization communications scheduled on a per base cycle basis in a communication period that is longer than the base cycle.

[0017]

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A second invention described in claim 2 provides the master/slave synchronization communication system wherein as the detecting section of the synchronization point, the master determines an arbitrary base cycle as a

5   synchronization point, and transmits instruction data to each slave based on the base cycle, and each of the slaves corrects a current value of the base cycle counter based on the base cycle counter value assumed when the instruction data is received and the pre-allocated base cycle counter

10 value assumed when the instruction data is received, and detects a time as a synchronization point when the count value reaches a predetermined value. As a result, all the stations are kept synchronous even when the communication period between the master and the slave is an integral

15 multiple of a base cycle.

[0018]

A third invention described in claim 3 provides the master/slave synchronization communication system wherein as a separate detecting section for the synchronization

20 point, the master determines an arbitrary base cycle as a synchronization point, and writes CYCLE_TIME register value as the next synchronization point in the instruction data when the master transmits instruction data to each slave based on the base cycle, and each of the slaves corrects a

25 current value of the base cycle counter value based on the

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CYCLE_TIME register value as the next synchronization point in the instruction data assumed when the instruction data is received and the current register value of its own CYCLE_TIME register value, and detects a time as a

5   synchronization point when the count value reaches a predetermined value. As a result, all the stations are kept synchronous even when the communication period between the master and the slave is an integral multiple a base cycle, by using a method different from the second

10   invention.

[0019]

A fourth invention described in claim 4 provides the master/slave synchronization communication system wherein as a separate detecting section for the synchronization

15   point, the master determines an arbitrary base cycle as a synchronization point, sets the base cycle counter value to a predetermined value, and transmits the present base cycle counter value to each slave when the master transmits an instruction to the each slave, and each of the slaves sets

20   the base cycle counter value to its own base cycle counter, and detects a time as a synchronization point when the count value reaches a predetermined value. As a result, all the stations are kept synchronous even when the communication period between the master and the slave is an

25   integral multiple a base cycle, by using a method different

from claims 2 and 3 of the invention.

[0020]

A fifth invention described in claim 5 provides the master/slave synchronization communication system wherein as a separate detecting section for the synchronization point, the master detects a synchronization point based on CYCLE_TIME register value, and simultaneously sets the base cycle counter value to a predetermined value, and each of the slaves detects a synchronization point based on the CYCLE_TIME register value by way of the same way as the master, and simultaneously sets the base cycle counter value to a predetermined value. As a result, all the stations are kept synchronous even when the communication period between the master and the slave is an integral multiple a base cycle, by using a method different from the second through four inventions.

[0021]

By detecting a synchronization point and executing transmission in accordance with a transmission schedule pre-registered in the transmission management table in synchronization with the synchronization point, data transmission/reception between a master and slaves is allowed even when the communication period between the master and a slave is an integral multiple a base cycle.

[0022]

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Advantages of the Invention

As mentioned above, according to the invention, it is possible to use a natural period as a base cycle and synchronize base cycle counters for counting the number of

5 cycles across all stations to implement a communication period that is an integral multiple of the natural period. By scheduling the transmission timing of instruction data from the master to slaves and response data from a slave to the master based on the synchronized base cycle counter

10 value, it is possible to provide a master/slave synchronization communication system capable of transmitting data while synchronizing all stations with a communication period that is an integral multiple of the natural period in a real-time control system to which

15 IEEE1394 is applied.

[0023]

For example, by using the method shown in Fig. 3 and setting a transmission management table and transmission timing information so that the transmission timing of

20 instruction data from the master to slaves and the transmission timing of response data from a slave to the master are paired and data is transmitted/received in the same base cycle, it is possible to perform scheduling of a polling system equivalent to PROFIBUS-DP in the related art

25 shown in Fig. 12 on the communication traffic in each base

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cycle in a communication period.

[0024]

For example, by using the method shown in Fig. 4 and setting a transmission management table and transmission timing information so that the transmission timing of response data from each slave to the master is in a separate base cycle delayed from reception of instruction data from the master to each slave, it is possible to perform scheduling of in each base cycle of the communication period in accordance with SERCOS as shown in Fig. 13.

[0025]

Also for cases other than those in Figs. 3 and 4 it is possible to readily implement desired master/slave synchronization communications by setting the transmission management table on the master side and the transmission timing information on the slave side.

Brief Description of the Drawings

[0026]

Fig. 1 is a system block diagram where IEEE1394 is applied in a fourth embodiment of the invention;

Fig. 2 shows an example of implementation of a master transmission management table and slave transmission timing information in an embodiment of the invention;

Fig. 3 is a communication timing chart in a second embodiment of the invention;

Fig. 4 is a communication timing chart in a third embodiment of the invention;

Fig. 5 is a CYCLE_TIME register of IEEE1394;

Fig. 6 is a flowchart of master instruction transmission processing in a first embodiment of the invention;

Fig. 7 is a flowchart of slave response transmission processing in the first embodiment of the invention;

Fig. 8 is a flowchart of the operation of a synchronization point detecting section of a slave in the second embodiment of the invention;

Fig. 9 is a flowchart of the operation of the synchronization point detecting section of a slave in the third embodiment of the invention;

Fig. 10 is a flowchart of the operation of the synchronization point detecting section of a slave in the fourth embodiment of the invention;

Fig. 11 is a flowchart of the operation of the synchronization point detecting section of a master and a slave in a fifth embodiment of the invention;

Fig. 12 is a communication timing chart showing an example of a related art method; and

Fig. 13 is a communication timing chart showing an

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example of another related art method.

[0027]

<u>Description of The Reference</u>

1   Master

2i   Slave

3   Transmission path of IEEE1394

10j   CYCLE_TIME register

11j   Cycle_synch

12j   Base cycle counter

130   Transmission management table

14j   Synchronization point detecting section

150   Instruction transmission processing

23i   Transmission timing information

25i   Response transmission processing

ci   Instruction data from slave #i

ri   Response data to slave #i

where $i=1, 2, … n$ ("n" is an integer of 1 or more.)

$j=0, 1, 2, … n$ ("n" is an integer of 1 or more.)

Detailed Description of the Preferred Embodiments

[0028]

Specific embodiments of the invention will be described based on drawings.

[0029]

[First Embodiment]

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First of all, feature names and signal names specified in the IEEE1394 Standard that appear in the following description will be described. As shown in Fig. 5, the CYCLE_TIME resister is composed of a cycle_offset part, a cycle_count part and a second_count part. The cycle_offset part counts a clock of 24.576Hz in each station. When the count reaches 3072, the cycle_offset part outputs a carry every $125\mu s$ of a natural period. The cycle_count part counts carries from the cycle_offset part. When the count reaches 8000, the cycle_offset part outputs a carry every 1s. Cycle_sync is a synchronization signal issued every $125\mu s$ of a natural period.

[0030]

Fig. 1 shows a specific embodiment of the first invention where reference 1 represents a master, reference 2i (i=1, 2,...n) represents a slave, and reference 3 represents a transmission path of IEEE1394. Reference 10j (j=0, 1,...n) represents a CYCLE_TIME register serving as a clock part of the master and each slave. From the CYCLE_TIME register 10j, Cycle_Synch 11j as a synchronization signal is output per natural period to count up the base cycle counter 12j. Cycle_Synch 11j also serves as an execution timing for a synchronization point detecting section 14j.

[0031]

The synchronization point detecting section 14j thus detects a synchronization point every time the base cycle counter is counted up and resets the base cycle counter value to 0 in case a synchronization point is detected.

5 With this, the values of the base cycle counters of all stations on a field network system may count up in synchronization.

[0032]

The master 1 owns a transmission management table

10 130. Based on the information from the transmission management table 130, an instruction transmission processing 150 transmits an instruction. Each slave i owns transmission timing information 23i and a response transmission processing 25i transmits response data based

15 on this information.

[0033]

Fig. 2 shows an embodiment of the transmission management table 130 on the master side and transmission timing information 23i on each slave. The transmission

20 management table on the master side stores destination slaves to which an instruction is to be transmitted for each base cycle value. The transmission timing information on each slave stores a base cycle value for which an instruction is to be received from the master and a

25 response is to be returned to the master.

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[0034]

Fig. 6 shows a processing flow of the instruction transmission processing 150 on the master side in Fig. 1 of the first embodiment. Fig. 7 shows a processing flow of the response transmission processing 25i on the slave side. Data transmission/reception according to the first invention will be sequentially described.

[0035]

As shown in Fig. 6, the master instruction transmission processing 150 is activated by Cycle_synch 110 per natural period and sets the value of a base cycle counter 120 to a read variable p at S1000. Next, at S1001, the master instruction transmission processing 150 sets the transmission instruction number as row data whose cycle counter value in the master transmission management table 130 corresponds to the variable p to the variable q and sets the list data of a corresponding destination slave number to an array variable $S[k]$ ($K=0$, $1,…,$ $q-1$). Then execution proceeds to loop processing between S1002 and S1004. At S1003 the master instruction transmission processing 150 transmits instruction data to a slave $S[k]$. In this way, operation may be such that every time the value of the base cycle counter 120 is updated, instruction data is transmitted to all slaves 2i to which transmission is scheduled in the cycle.

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[0036]

As shown in Fig. 7, the slave response transmission processing 25i is activated by Cycle_synch per natural period and sets the value of a base cycle counter 12j to the read variable p at S2000. Next, the slave response transmission processing 25i compares the response cycle value in the transmission timing information 23i with the variable p and, in case a match is found, transmits response data because the cycle is a response cycle. Otherwise, the slave response transmission processing 25i does not transmit response data because the cycle is not a response cycle. In this way, it is possible to operate so as to transmit response data every time a pre-scheduled value of the base cycle counter 12i is reached.

[0037]

As such, it is possible for the master 1 and slaves 2i to perform communications in synchronization with respective scheduled timings in accordance with the value of the base cycle counter 12j.

[0038]

Fig. 3 is a communication timing chart where the transmission/reception table and transmission timing information are scheduled so as to complete transmission/reception in the same base cycle. By properly setting the master transmission management table 130 and

the slave transmission timing information 23i and for example assuming destination slave No. in the row of the cycle counter value 0 in the master transmission management table 130 as #1, #2, destination slave No. 3 in the row of

5   the cycle counter value 1 as #3, #4 as well as setting each response cycle value of the transmission timing information 23i in the slaves #1, #2 to 0 and setting each response cycle value of the transmission timing information 23i in the slaves #3, #4 to 1, instruction data to the slaves #1

10   and #2 is transmitted when the value of the base cycle counter 12j is 0 and response data from the slaves #1 and #2 is returned. Similarly, it is possible to transmit/receive instruction data and response data as a data pair of an arbitrary slave 2i in the same base cycle.

15   [0039]

Fig. 4 is a communication timing chart where the transmission/reception table and transmission timing information are scheduled so as to transmit a response in the same base cycle. By properly setting the master

20   transmission management table 130 and the slave transmission timing information 23i and for example assuming destination slave No. in the row of the cycle counter value 0 in the master transmission management table 130 as #1, #2, destination slave No. 3 in the row of the

25   cycle counter value 1 as #3, #4 as well as setting each

response cycle value of the transmission timing information

23i in the slaves #1, #2 to 4 and setting each response

cycle value of the transmission timing information 23i in

the slaves #3, #4 to 5, instruction data to the slaves #1

5   and #2 is transmitted when the value of the base cycle

counter 12j is 0 and response data from the slaves #1 and

#2 is returned with a delay of four cycles, when the value

of the base cycle counter 12j is 4. Similarly, scheduling

may be made so that instruction data to the slaves #3 and

10   #4 is transmitted when the value of the base cycle counter

12j is 1 and response data from the slaves #3 and #4 is

returned with a delay of four cycles, when the value of the

base cycle counter 12j is 5.

[0040]

15   [Second Embodiment]

Next, an embodiment of the synchronization point

detecting section 14j that synchronizes the updates of the

base cycle counter 12j will be described. As a matter of

fact, detection of a synchronization point is made

20   individually for the master 1 and each slave 2i and the

result is reflected on the value of the base cycle counter

12j of each station. A cycle that serves as its

synchronization point requires the same determination

result by all stations. While the value of the base cycle

25   counter 12j is 0 at this synchronization point and

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thereafter the value of the base cycle counter 12j is incremented every time a base cycle elapses, that is, the Cycle_synch event 11j takes place and the value of the base cycle counter 12j returns to 0 at the next synchronization point after a predetermined communication period has elapsed in this embodiment, transition of the value of the base cycle counter 12j is not limited thereto but the value may be decremented. A base cycle counter value at a synchronization point need not be 0 as long as it is a specified value.

[0041]

A second invention that is a specific method of the synchronization point detecting section 14j will be described. In a synchronization point detection processing 140 of the master 1, a synchronization point detecting section is activated by a Cycle_synch event 11j per natural period and only increments the base cycle counter 120 and determines whether the value is 0.

[0042]

Processing at each slave 2i will be described in line with Fig. 8. First, the processing determines whether instruction data from the master 1 is received in the last base cycle at S3000. In case the data is received, recognizing that the last base cycle is an instruction cycle in the transmission timing information, the

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processing sets the value of an instruction cycle value plus 1 as a current base cycle counter value. Otherwise, the processing increments the base cycle counter 12j at S3005. In case the base cycle counter value updated for wraparound determination is equal to or more than the total number of cycles in the transmission timing information 23i at S3002, the processing resets the count value to 0 at S3003. Recognizing that the current cycle is a synchronization point, the processing performs necessary synchronization point detection processing at S3004.

[0043]

[Third Embodiment]

A third invention that is another method for the synchronization point detection processing 14j will be described. In a synchronization point detection processing 140 of the master 1, a synchronization point detecting section is activated by a Cycle_synch event 11j per natural period and only increments the base cycle counter 120 and determines whether the value is 0. The instruction data transmitted from the master to each slave in accordance with the transmission management table includes the CYCLE_TIME register value at the next synchronization point.

[0044]

Processing at each slave 2i will be described in line

with Fig. 9. First, the processing determines whether instruction data from the master 1 is received in the last base cycle at S4000. In case the data is received, the processing extracts at S4001 the CYCLE_TIME register value

5   as the next synchronization point in the received instruction data. Next, at S4002, the processing obtains the difference between the cycle_count value of the current CYCLE_TIME register and the cycle_count value of the next synchronization point CYCLE_TIME register in the

10   instruction data. At S4003, the processing obtains the residue of the result of dividing {(total number of cycles in the slave transmission timing information 23i)-(the difference) by (total number of cycles in the slave transmission timing information 23i) and sets the obtained

15   value as a current base cycle counter value. For example, in case the cycle_count value of the next synchronization point CYCLE_TIME register is 45, the cycle_count value of the current CYCLE_TIME register is 43, and total number of cycles is 6, {6-(45-43)}÷6=residue of 4÷6=4. The value 4

20   is set to the base cycle counter. Otherwise, the processing increments the base cycle counter 12j at S4007. In case the base cycle counter value updated for wraparound determination is equal to or more than the total number of cycles in the transmission timing information 23i at S4004,

25   the processing resets the count value to 0 at S4005.

Recognizing that the current cycle is a synchronization point, the processing performs necessary synchronization point detection processing at S4006.

[0045]

5 [Fourth Embodiment]

A fourth invention that is another method for the synchronization point detection processing 14j will be described. In a synchronization point detection processing 140 of the master 1, a synchronization point detecting

10 section is activated by a Cycle_synch event 11j per natural period and only increments the base cycle counter 120 and determines whether the value is 0. The instruction data transmitted from the master to each slave in accordance with the transmission management table includes the then

15 master base cycle counter value.

[0046]

Processing at each slave 2i will be described in line with Fig. 10. First, the processing determines whether instruction data from the master 1 is received in the last

20 base cycle at S5000. In case the data is received, the processing sets the value of a base cycle value included in the instruction data plus 1 to the base cycle counter of the slave. Otherwise, the processing increments the base cycle counter 12j at S5005. In case the base cycle counter

25 value updated for wraparound determination is equal to or

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more than the total number of cycles in the transmission timing information 23i at S5002, the processing resets the count value to 0 at S5003. Recognizing that the current cycle is a synchronization point, the processing performs

5 necessary synchronization point detection processing at S5004.

[0047]

[Fifth Embodiment]

A fifth invention that is another method for the

10 synchronization point detection processing 14j will be described referring to Fig. 11. In a synchronization point detection processing 140 of the master 1, a synchronization point detecting section is activated by a Cycle_synch event 11j per natural period. The synchronization point

15 detection processing 14j determines whether the cycle_count value of the CYCLE_TIME register is divisible by the total number of base cycles necessary for a communication period. In case it is divisible, the synchronization point detection processing 14j assumes a synchronization point,

20 sets the base cycle counter value to 0 at S6001 and performs necessary synchronization point detection processing at S6002. Otherwise, the synchronization point detection processing 14j determines that the current cycle is not a synchronization point and increments the

25 cycle_count value of the CYCLE_TIME register at S6003.

Instead of incrementing the base cycle, the synchronization point detection processing 14j may set the residue of the result of dividing the cycle_count value of the CYCLE_TIME register by the total number of cycles of base cycles necessary for a communication period to the base cycle counter.

[0048]

The each slave can detect a synchronization point by using the same way as the master based on the CYCLE_TIME register value of each slave.

[0049]

<Industrial Applicability>

In this way, it is possible to implement a real-time control system capable of master/slave synchronization communications by using IEEE1394 for communications between a master and a slave, the real-time control system including a master 1 shown in Fig. 1 as a controller and a slave 2i as a device controlled by the controller in a fixed period. As a specific example, there is provided a motion control system where the master is composed of motor drive devices such as a motion controller.